



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:

Yoshimasa SEKINO

Serial No. 10/811,836

Filed: 3/30/2004

For: POWER-ON RESET CIRCUIT

)
) Group Art Unit: 2816
) Examiner: Terry D. Cunningham
) Confirmation: 3050
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AMENDMENT PURSUANT TO 37 C.F.R. §1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to issuance, please amend the above identified application as follows:

IN THE CLAIMS:

Please amend claim 3 as follows.

3. (Currently Amending) A power-on reset circuit comprising:
a first capacitor connected between a power supply line and a first node;
a first MOS transistor connected between said first node and a second node, and
ON/OFF controlled based on a first pulse signal;
a second MOS transistor connected between said second node and a reference
potential, and ON/OFF controlled based on a second pulse signal;
a second capacitor connected between said second node and said reference potential;
a timing control unit for generating said first and second pulse signals in synchronism
with a clock signal externally applied thereto; and
an output portion outputting a reset signal when the potential of said internal node an
internal node decreases below a threshold voltage after the application of a power supply
voltage to said power supply line.